REMARKS

Claim 8 has been rejected under 35 U.S.C. 112, second paragraph for failing to provide proper antecedent basis for the recited "nitride layer". The Applicant has amended Claim 8 to properly recite an "intermediate dielectric layer", thereby providing proper antecedent basis for this claim.

Claims 9-11, which depend from Claim 8, meet the requirements of 35 U.S.C. 112, second paragraph in view of the amendment to Claim 8.

Claim 15 has been rejected under 35 U.S.C. 112, second paragraph for failing to provide proper antecedent basis for the recited "top dielectric layer". The Applicants have amended Claim 15 to recite "depositing a top dielectric layer over the intermediate dielectric layer", thereby providing proper antecedent basis for this claim.

Claim 7 has been objected to as being independent upon a rejected base claim. The Examiner has indicated that this claim would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The Applicants have amended Claim 7 in accordance with the Examiner's suggestion, thereby rendering Claim 7 (and dependent Claims 8-11) allowable.

Claims 1-6 and 12 have been rejected under 35 U.S.C. 102 as being anticipated by Lu et al. (U.S. Patent 5,963,808).[1]

Claim 1 recites "forming one or more diffusion bit line regions in a semiconductor substrate". The Examiner indicates that Lu et al. teach this step in Fig. 9B, wherein diffusion bit lines 212, 214 and 216 are formed.

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[1] The language of the Office Action erroneously replicates the prior rejection of Claims 1-12 and 15 in view of Ohtani et al.

Claim 1 further recites "then thermally oxidizing the upper surface of the semiconductor substrate, thereby forming a bottom oxide layer over the upper surface of the semiconductor substrate and simultaneously forming bit line oxide regions over each of the one or more diffusion bit line regions".

The Examiner indicates that Lu et al. teach this step in Fig. 10A, wherein thermal oxide regions 1000a, 1000b and 1000c are formed over diffusion bit line 212, 214 and 216. However, while Lu et al. may teach the formation of thermal oxide regions over diffusion bit lines bit lines, Lu et al. fail to teach the simultaneous formation of a bottom oxide layer over the upper surface of the semiconductor substrate. In fact, Lu et al. explicitly teaches that silicon oxide layer 404 is formed before either the diffusion bit lines 212, 214 and 216 or the thermal oxide regions 1000a, 1000b and 1000c. For these reasons, Lu et al. fail to teach "forming a bottom oxide layer … and simultaneously forming bit line oxide regions" as recited by Claim 1. For this reason, Claim 1 is not anticipated by Lu et al. Claims 2-6 and 12, which depend from Claim 1, are not anticipated by Lu et al. for at least the same reasons as Claim 1.

Claims 13 and 14 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Lu et al.

Claims 13-14, which depend from Claim 1, are allowable over Lu et al. for at least the same reasons as Claim 1.

The Applicants have added new Claim 16, which recites "The method of Claim 1, wherein the intermediate dielectric layer is formed directly on the bottom oxide layer and the bit line oxide regions". Support for this claim appears in the specification as originally filed in paragraph [0043] and in Fig. 8. No new matter is added. (Note that elements

800a-800b and 700a-700b of Lu et al. cannot possibly correspond with the "intermediate dielectric layer" of Claim 16 (or Claim 1), because these elements of Lu et al. are formed prior to forming the diffusion bit line regions 212, 214 and 216, and prior to forming thermal oxide regions 1000a-1000c.)

CONCLUSION

Claims 1-16 are pending in the present application. Claims 7-11 are allowable. Reconsideration and allowance of Claims 1-6 and 12-16 is respectfully requested. If there are any questions, please telephone the undersigned at (925) 895-3545 to expedite prosecution of this case.

Respectfully submitted,

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